PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 0057-013PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2007/004031	International filing date *(day/month/year)* 16 February 2007 (16.02.2007)	Priority date *(day/month/year)* 16 February 2006 (16.02.2006)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant VNS PORTFOLIO LLC		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

   - ☒ Box No. I — Basis of the report
   - ☐ Box No. II — Priority
   - ☐ Box No. III — Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - ☐ Box No. IV — Lack of unity of invention
   - ☒ Box No. V — Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - ☐ Box No. VI — Certain documents cited
   - ☐ Box No. VII — Certain defects in the international application
   - ☐ Box No. VIII — Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 19 August 2008 (19.08.2008)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Yolaine Cussac e-mail: pt05.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	07 JUL 2008
Applicant's or agent's file reference 0057-013PCT	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US07/04031	16 February 2007 (16.02.2007)	16 February 2006 (16.02.2006)

International Patent Classification (IPC) or both national classification and IPC

IPC: **G06F 15/163**(2006.01) G06F 15/80(2006.01)
USPC: 712/10,712/32,712/202

Applicant

CHARLES MOORE

1. This opinion contains indications relating to the following items:

- ☒ Box No. I — Basis of the opinion
- ☐ Box No. II — Priority
- ☐ Box No. III — Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV — Lack of unity of invention
- ☒ Box No. V — Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI — Certain documents cited
- ☐ Box No. VII — Certain defects in the international application
- ☐ Box No. VIII — Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis(b)* that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/ US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	23 May 2008 (23.05.2008)	Henry Tsai Telephone No. (571)272-9772

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US07/04031

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - ☒ the international application in the language in which it was filed
   - ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))
3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material
      - ☐ a sequence listing
      - ☐ table(s) related to the sequence listing

   b. format of material
      - ☐ on paper
      - ☐ in electronic form

   c. time of filing/furnishing
      - ☐ contained in the international application as filed.
      - ☐ filed together with the international application in electronic form.
      - ☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US07/04031

Box No. V Reasoned statement under Rule 43 *bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims NONE	YES
	Claims 1-25	NO
Inventive step (IS)	Claims NONE	YES
	Claims 1-25	NO
Industrial applicability (IA)	Claims 1-25	YES
	Claims NONE	NO

2. Citations and explanations:

Please See Continuation Sheet

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US07/04031

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

V. 2. Citations and Explanations:

Claims 1-25 lack novelty under PCT Article 33(2) as being anticipated by Intel® (Enhanced Serial Port on the 83C51FA, 1987), hereinafter referring to as Intel.

Referring to claim 1, Intel discloses a computer array (page 1, left col., lines 18-20; multiple MCS®-51 based controllers; and page 2, left col., line 54; Note: the MCS is also known or referred as Micro Computer Systems), comprising:

a plurality of computers (page 2, right col., lines 43-46; slave and master); and

a plurality of data paths (pages 3-4, listings 1-3 show slave and master computers with receiving/transmitting data path and controlling routines) connecting the computers; and wherein

when a first one of said computers (page 2, right col., line 50, and listings 1-2, slave computer receiving routine) attempts a communication (pages 3-4, listings 1-3, serial port receiving/transmitting communication and their initialization) with a second one of said computers (page 4, left col., line 15, and listing 3, master computer transmitting routine) then said first one of said computers (page 2, right col., line 50, and listings 1, 2; the slave computer) stops operation until said second one of said computers (page 4, left col., line 15, and listing 3; the master computer) is ready to complete the communication (page 3, listing 2, line 15; when the receiving from master transmitting, the RI will be set automatically as master completed the communication, then to initiate another communication, the RI needs to be cleared as by CLR RI; please also refer to the pages 9-4 of 8XC251SB Embedded Microcontroller User's Manual for explanation of RI and TI if necessary for referenced inherency usage).

Referring to claim 9, Intel discloses a method for communicating between (page 2, right col., lines 43-46; slave and master) a first computer device and a second computer device, comprising:

causing the first computer device (page 2, right col., line 50, and listings 1-2; slave computer receiving routine) to indicate its readiness to communicate with the second computer device (page 4, left col., line 15, and listing 3; master computer transmitting routine);

causing (page 3, listing 2, line 15, CLR RI shows the readiness; when the receiving from master transmitting, the RI will be set automatically as master completed the communication, then to initiate another communication, the RI needs to be cleared as by CLR RI; please also refer to the pages 9-4 of 8XC251SB Embedded Microcontroller User's Manual for explanation of RI and TI if necessary for referenced inherency usage) the second computer device to indicate its readiness to complete the communication;

transferring (pages 3-4, listings 1-3; receiving/transmitting communication and their initialization) data between the first

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US07/04031

Supplemental Box
In case **the space in any of the preceding boxes is not sufficient.**

computer device and the second computer device; and
causing (page 3, listing 2, line 16, and page 4, lines 6-14, SETB SM2 to re-enable as acknowledge next new communication addressing) the second computer device to acknowledge to the first computer device that the communication is completed.

Referring to claim 17, Intel discloses a method for communicating between computers (page 2, right col., lines 43-46; slave and master), comprising:
(a) causing a first computer to indicate its readiness to communicate (page 4, listing 3, initializing master for communication);
(b) causing said first computer to then cease operation (page 4, listing 3, CLR TI for next transmission; note, prior CLR TI, the TI was set, and computer was not in transmitting operation);
(c) causing a second computer to indicate its readiness (page 3, listing 2, line 15, CLR RI shows the readiness) to communicate to said first computer;
(d) transferring data (pages 3-4, listings 1-3; receiving/transmitting communication and their initialization) between said first computer and said second computer; and
(e) causing (page 3, listing 2, line 16, and page 4, lines 6-14, SETB SM2 to re-enable as acknowledge next new communication addressing) said first computer to resume operation.

Referring to claim 24, Intel discloses a computer, comprising:
at least one data transmission means (page 2, right col., lines 43-46; slave and master) for communicating between a first computer and a second computer;
means for causing said first computer to indicate that it is ready to communicate (page 4, listing 3, initializing master for communication);
means for stopping (page 3, listing 2, line 15, CLI RI together with page 4, list 3, CLR TI) said first computer until said second computer indicates that it is ready to communicate;
means for causing said second computer to indicate that it is ready to communicate (page 3, listing 2, line 15, CLR RI shows the readiness);
means for acknowledging (page 3, listing 2, line 16, and page 4, lines 6-14, SETB SM2 to re-enable as acknowledge next new communication addressing) that a communication has been accomplished.

As to claim 2, Intel discloses the computer array of claim 1, wherein:
said first of said computers (page 4, left col., line 15, and listing 3; the master computer) is attempting to write (page 4, left col., line 15, and listing 3; the master computer initialized for attempting to transmit); and
said second one of said computers (page 2, right col., line 50, and listings 1-2; the slave computer) completes the communication by reading (page 2, right col., line 50, and listings 1-2; the slave computer receiving from master) from said first one of said computers.

As to claim 3, Intel discloses the computer array of claim 1, wherein:
said first one of said computers (page 2, right col., line 50, and listings 1-2, the slave computer) is attempting to read (page 2, right col., line 50, and listings 1-2; the slave computer receiving as reading from master); and
said second one of said computers (page 4, left col., line 15, and listing 3, the master computer) completes the communication by writing (page 4, left col., line 15, and listing 3, the master computer completes writing to slave as transmit causes TI to be set at master and RI set at slave computer) to said first one of said computers.

As to claim 4, Intel discloses the computer array of claim 2, wherein:
said first one of said computers (page 1, right col., lines 37-38, the master computer configured to read as communicate with group of slaves) is configured to read from more than one other computer.

As to claims 5 and 22, Intel discloses the computer array of claim 1, wherein:
when the first one of said computer (page 1, right col., lines 37-38, the master computer) attempts a communication with the second of said computers then the first computer sets a write line high (page 4, listing 3, line 21, "JNB TI,$" as a busy loop indicates the write line "transmit interrupt – TI" remains high while transmitting by MOV SBUF, #MESSAGE_1); and
when the second one of said computers (page 2, right col., line 50, and listings 1-2, the slave computer) is ready to complete the communication it sets a read line high (page 3, listing 2, line 15; the receiving slave has RI setting high during receiving as ready and working on complete the communication, the communication is done by MOV TEMP, SBUF in listing 2, line 13; and the CLR RI means to wait for next asynchronous receiving transmission).

As to claims 6 and 20, Intel discloses the computer array of claim 5, wherein:
when the read line is high and further when the corresponding write line is also high then data is transferred between (pages 3-4, listings 2-3; the transmitting master sending data will keep the TI set, at the same time the receiving slave receiving data will keep the RI set, so communication is ongoing when both are set until they are set by CLR TI, CLR RI command) the first one of said computers and the second one of said computers.

As to claims 7, 15 and 21, Intel discloses the computer array of claim 6, wherein:
when data is transferred between the first one of said computers and the second one of said computers, then the read line and

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US07/04031

Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

the write line both go low (pages 3-4, listings 2-3; TI will be clear after the transmitting master completed, at the same time the RI will be clear after receiving slave completed, so both are set to low).

As to claims 8, 16 and 18, Intel discloses the computer array of claim 7, wherein:
when the read line and the write line both go low (pages 3-4, listings 2-3; TI will be clear after the transmitting master completed, at the same time the RI will be clear after receiving slave completed, so both are set to low), then both the first one of said computers and the second one of said computers resume operation (pages 3-4, listings 2-3; cleared TI initialized another transmitting, cleared RI initialized another receiving).

As to claim 10, Intel discloses the method of claim 9, wherein:
the first computer device indicates its readiness (page 4, left col., line 15, and listing 3; the master computer initialized for attempting to transmit) to write to the second computer.

As to claim 11, Intel discloses the method of claim 10, wherein the first computer device indicates its readiness to write to the second computer by setting a write line (page 4, left col., line 15, and listing 3; the master computer initialized for attempting to transmit) between the first computer and the second computer to high.

As to claim 12, Intel discloses the method of claim 9, wherein:
the first computer device indicates its readiness (page 2, right col., line 50, and listings 1-2; the slave computer receiving as reading from master) to read from the second computer.

As to claim 13, Intel discloses the method of claim 12, wherein the first computer device indicates its readiness to read from the second computer by setting a read line (page 2, right col., line 50, and listings 1-2; the slave computer receiving as reading from master) between the first and second computer to high.

As to claims 14 and 19, Intel discloses the method of claim 9, wherein:
the first computer device indicates its readiness to communicate with the second computer device by setting one of a read line (page 2, right col., line 50, and listings 1-2; the slave computer receiving as reading from master) or a write line (page 4, left col., line 15, and listing 3; the master computer initialized for attempting to transmit) to high;
the second computer device indicates its readiness to communicate with the first computer device by setting the other of the read line or the write line to high (page 4, left col., line 15, and listing 3, the master computer completes writing to slave as transmit causes TI to be set at master and RI set at slave computer); and
when both the read line and the write line are high (pages 2-4, listing 1-3) then data is transferred between the first computer device and the second computer device.

As to claim 25, Intel discloses the computer of claim 24, and further including means for stopping (page 4, left col., line 15, and listing 3, the master computer completes writing to slave as transmit causes TI to be set at master and RI set at slave computer) said first computer until said means for acknowledging that a communication has been accomplished has so indicated.

Claims 1-25 meet the criteria set out in PCT Article 33(4), and thus meet industrial applicability because the subject matter claimed can be made or used in industry.